REMARKS

Claims 1-20, all the claims pending in the application, stand rejected on prior art grounds. Applicants respectfully traverse these rejections based on the following discussion.

I. The Prior Art Rejections

Claims 1-7 stand rejected under 35 U.S.C. §102(b) as being anticipated by Temple, et al. (U.S. Patent No. 5,654,226), hereinafter referred to as Temple. Claims 1-16 and 18-20 stand rejected under 35 U.S.C. §102(b) as being anticipated by Delgado, et al. (U.S. Patent No. 5,091,331), hereinafter referred to as Delgado. Claims 13, 10, and 17 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Delgado, in view of Yoshihara, et al. (U.S. Patent No. 6,555,901), hereinafter referred to as Yoshihara. Applicants respectfully traverse these rejections based on the following discussion.

A. Rejection of Claims 1-7 under 35 U.S.C. §102(b) based on Temple

More particularly, the Applicants respectfully traverse the rejection of independent claim 1 based on Temple because Temple does not teach or suggest the following patentable features: (1) providing a supporting wafer that has a planar surface and oxide regions at that planar surface, (2) a limited number of joining points corresponding to the oxide regions at the planar surface of the supporting wafer, and (3) during the cutting process, the integrated circuit wafer separates from the supporting wafer in chip sections.

Temple teaches a method of processing wafers in which a device wafer 12 is selectively bonded to a carrier wafer 10 in order to support the device wafer during processing (see column 2, line 62 – column 3, line 2). Figures 2A-F illustrate exemplary bonds 20 that may be formed in areas 18 between the carrier wafer 10 and the silicon wafer 12. In each of the exemplary embodiments bonds 20 extend between the two wafers 10, 12 in selected areas such that spaces are also formed between the two wafers (see Figures 2A-F and column 3, lines 11-55). Once processing is completed on the front surface of the device wafer, the bonded device/carrier wafer is cut completely through along saw lines so that dies are formed from cut sections of the device wafer where the two wafers were not joined (see column 4, lines 49-51).

Contrarily, the present invention first provides a supporting wafer that has a planar surface and discrete oxide regions at the planar surface (see paragraph [0035] and Figure 4; see also paragraph [0036] and Figure 7). These oxide regions are located within the supporting wafer itself and are exposed at the upper surface of the supporting wafer which is planar. The integrated circuit wafer is partially joined to the supporting wafer at a limited number of joining points. These joining points correspond to the exposed oxide regions (see paragraphs [0037-0039] and Figures 8-10). Since additional material does not have to be added to the surface of either the supporting wafer or the integrated circuit wafer to form the bond little or no space is formed between the two wafers (see Figure 10). After processing the integrated circuit wafer, either both wafers that are bonded together are cut through to form chip sections as well as cut sections of the supporting wafer (see Figure 12) or the integrated circuit wafer alone is cut through

and the integrated circuit wafer separates from the supporting wafer in chip sections (see Figure 14).

Those skilled in the art will recognize that avoiding the spaces between the two wafers increases mechanical strength in order to avoid local wafer warpage (e.g., wafer warpage caused by mismatch of thermal expansion coefficient during high temperature process). Additionally, those skilled in the art will recognize that avoiding the spaces between the two wafers allows for more accurate and efficient cutting to form chip sections (dies) because as the partially bonded device/carrier wafer of Temple is cut through and selected bonds are removed support area for dicing can become insufficient.

Therefore, amended independent claim 1, is patentable over Temple. Further, dependent claims 2-7 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. Moreover, the Applicants note that claims 1-7 are properly supported in the specification and accompanying drawings, and no new matter is being added. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

B. Rejection of Claims 1-16 and 18-20 under 35 U.S.C. §102(b) based on Delgado

More particularly, the Applicants respectfully traverse the rejection of independent claims 1, 8, and 15 based on Delgado because Delgado does not teach or suggest the following patentable features: (1) providing a supporting wafer that has a

planar surface and oxide regions at that planar surface, (2) a limited number of joining points corresponding to the oxide regions at the planar surface of the supporting wafer, and (3) during the cutting process, the integrated circuit wafer separates from the supporting wafer in chip sections.

Delgado teaches a method of fabricating a wafer that incorporates bonding a pair of wafers together in order to perform wafer thinning and formation steps on one of the wafers and, particularly, a method for dicing thin wafers (see column 1, lines 7-10 and lines). Specifically, as described in column 3, lines 10-19, a wafer 10 is formed such that it has a surface with oxidized peaks 22 and valley regions 24. A handle wafer 30 is also formed such that it has a planar bonding surface 32 with an oxide bonding layer 40 covering the entire bonding surface. The two wafers 10 and 30 are pressed together and heated such that only the peaks 22 of wafer 10 bond with the surface of wafer 30. Alternatively, the surface of the handle wafer has the peaks and valleys (see column 3, lines 53-58). Once the two wafers are bonded, the thickness of wafer 10 can be reduced (see column 3, lines 20-25). Then, in order to dice the wafer 10, the wafer must first be mounted to sticky tape 30 so that proper support is achieved.

Contrarily, as mentioned above, the present invention first provides a supporting wafer that has a planar surface and discrete oxide regions at the planar surface (see paragraph [0035] and Figure 4; see also paragraph [0036] and Figure 7). The integrated circuit wafer is partially joined to the supporting wafer at a limited number of joining points that correspond to these oxide regions (see paragraphs [0037-0039] and Figures 8-10). Since no peaks or valleys are formed in either the integrated circuit wafer or the

supporting wafer, the bond between the two wafers is formed with little or no space is between the two wafers (see Figure 10). After processing the integrated circuit wafer, either both wafers that are bonded together are cut to form chip sections as well as cut sections of the supporting wafer (see Figure 12) or the integrated circuit wafer alone is cut through and the integrated circuit wafer separates from the supporting wafer in chip sections (see Figure 14).

As mentioned above avoiding the spaces between the two wafers increases mechanical strength in order to avoid local wafer warpage (e.g., wafer warpage caused by mismatch of thermal expansion coefficient during high temperature process). Additionally, because the method of the claimed invention avoids spaces (peaks and valleys) between the two wafers, the necessity of mounting the integrated circuit wafer on to sticky tape for support prior to dicing is also avoided.

Therefore, amended independent claims 1, 8 and 15 are patentable over Delgado. Further, dependent claims 2-7, 9-14 and 16-20 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. Moreover, the Applicants note that claims 1-20 are properly supported in the specification and accompanying drawings, and no new matter is being added. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

II. Formal Matters and Conclusion

With respect to the rejections to the claims, the claims have been amended, above, to overcome these rejections. In view of the foregoing, Applicants submit that claims 1-20, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0458.

Respectfully submitted,

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